REMARKS

The Office Action dated June 9, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. By this Amendment, claims 1, 9, 20, 23, 28, 30, 41, 42, 45, 46, 49, 50 and 51 have been cancelled. The subject matter of claim 51 has been incorporated into claim 52. Claim 52 is now in independent form. The subject matter of claims 1, 9, 20, 23, 28, 30, 41, 42, 45, 46, 49 has substantially been incorporated into newly added claims 53-64. Claims 2, 10, 19, 16, 18, 21, 24-47, 29, 31, 33-38, 43, 44, 47 and 48 have merely been amended to depend from the newly added independent claims. No new matter has been added or amendments made that narrow the scope of any elements of any claims. Accordingly, claims 2-8, 10-19, 21, 22, 24-27, 29, 31-40, 43, 44, 47, 48 and 52-64 are pending in this application and are submitted for consideration.

Applicants acknowledge and thank the Examiner for indicating that claims 4-6, 8, 12, 15, 19, 34, 40 and 44 would be allowable over the prior art if amended to be in independent form. However, Applicants respectfully submit that all of the presently pending claims recite allowable subject matter and therefore, placing claims 4-6, 8, 12, 15, 19, 34, 40 and 44 into independent form is not necessary.

Claims 1-3, 7, 9-11, 14, 16, 20-32, 35-38, 41-43 and 45 were rejected under 35 U.S.C. § 102(e) as being anticipated by Higuchi et al. (U.S. Patent No. 6,167,037, "Higuchi"). As discussed above, by this amendment, claims 1, 9, 20, 23, 28, 30, 41 and 42 have been cancelled and the subject matter incorporated into claims newly added 53-60. Claims 2, 3 and 7 depend from claim 53, claims 10, 11, 14 and 16 depend from

claim 54, claims 21-22 depend from claim 22, claims 24-27 depend from claim 56, claim 29 depends from claim 57, claims 31-32 and 35-38 depend from claim 58, and claim 43 depends from claim 60. Therefore, Applicants respectfully submit that claims 2, 3, 7, 10, 11, 14, 16, 21-22, 24-27, 31-32, 35-38, 43 and 53-60 recite subject matter that is neither disclosed nor suggested in Higuchi.

Claim 53 recites a cell search method comprising the steps of detecting correlation values between an input signal and a spreading code; comparing each of said detected correlation values with a threshold value; and detecting a correlation peak value in a predetermined unit of slots in accordance with a result of said comparison.

Claim 54 recites a communication synchronization apparatus including a detection device that detects correlation values between an input signal and a spreading code generated by the detection device, and detects a correlation peak value in a predetermined unit of slots to detect a synchronization point of said input signal. A comparison section is provided for comparing each of the detected correlation values with a predetermined threshold value.

Claim 55 recites a computer-readable storage medium for a communication synchronization apparatus including a detection device that detects correlation values between an input signal and a spreading code generated by the detection device, and detects a correlation peak value in a predetermined unit of slots to detect a synchronization point of said input signal, the medium stores a program for causing a computer to realize a comparison function of comparing each of the detected correlation values with a predetermined threshold value.

Claim 56 recites a cell search method comprising the steps of detecting correlation values between an input signal and a spreading code; comparing each of said detected correlation values with a threshold value; detecting a correlation peak value in a predetermined unit of slots in accordance with a result of said comparison; and ending the process when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count set value.

Claim 57 recites a cell search method comprising the steps of detecting correlation values between an input signal and a spreading code; comparing each of said detected correlation values with a threshold value; detecting a correlation peak value in a predetermined unit of slots in accordance with a result of said comparison; and providing a first mode in which the process is ended when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count set value, and a second mode in which the process is performed a predetermined number of times.

Claim 58 recites a communication synchronization apparatus including:

a detection device that detects each slot in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device, the detection process for correlation value is performed over several slots, the correlation values obtained in the slots are integrated to detect a correlation peak value, and thereby a synchronization point of said input signal is detected. A comparison section is provided for comparing each of a calculated integrated correlation value with a reference set value.

Claim 59 recites a communication synchronization apparatus including a detection device that detects each slot in a predetermined unit, correlation values between an input signal and a spreading code generated by the detection device, the detection process for correlation value is performed over several slots, the correlation values obtained in the slots are integrated to detect a correlation peak value, and thereby a synchronization point of said input signal is detected. A comparison section is provided for comparing each of the detected correlation value or each of a value output from a power conversion device for converting the correlation value into a power value, with a reference set value.

Claim 60 recites a communication synchronization apparatus including a detection device that detects each slot in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection process for correlation value is performed over several slots, the correlation values obtained in the slots are integrated to detect a correlation peak value, and thereby a synchronization point of said input signal is detected. A first mode is included in which integration is ended when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count set value, and a second mode in which integration is performed a predetermined number of times.

In making this rejection, the Office Action took the position that Higuchi discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the structure of the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, the present invention is configured to detect a correlation value between an input signal and

a spreading code, and detect a correction peak value in a predetermined unit of slots by comparison between each of the detected correlation value and threshold value.

As a result of the claimed configuration, in the correlation values obtained in a slot, the correlation values exceeding the threshold value are registered in the memory, and the correlation values not exceeding the threshold value are neglected as noise data. The unnecessary correlation values at noise levels are not stored in the memory. For this reason, the number of correlation values actually stored in the memory can be decreased. Hence, the necessary storage capacity of the memory can be greatly decreased, and so the physical circuit area of the memory can be considerably reduced.

The present invention includes detecting a correlation value between an input signal and a spreading code, and detecting a correlation peak value in a predetermined unit of slots by comparison between each of the detected correlation value and a threshold value.

As discussed at column 11, lines 31-37 of Higuchi, as shown in Fig. 9, the mobile station first carries out correlation detection between the received signal and the short code (first spreading code) used as the spreading code replica to detect the phase of the received long code (second spreading code) from the timing of the maximum peak at step S2000. It is further discussed in column 11, lines 46-48, that detected correlation values of respective long codes are stored in a memory at step S2200, and the maximum correlation value is selected at step S2300. As also discussed in column 11, lined 49-54, a threshold value decision is made for the maximum correlation value at step S2400. If the maximum correlation value exceeds the threshold value, a decision

is made that the present spreading code replica is the received spreading code, thus completing the spreading code synchronization.

However, the present invention compares each of the correlation value with the threshold value, as recited in claims 53-55, Higuchi appears to compare the maximum correlation value only with the threshold value. Additionally, the present invention detects the correlation peak value in the predetermined unit of slots by comparison between each of the correlation value and the threshold value, as recited in claims 53-55, whereas Higuchi compares the maximum correlation value with the threshold value after selecting the maximum correlation value.

Thus, in sum the present invention compares each correlation value with the threshold value to detect the maximum correlation value, whereas Higuchi compares the maximum correlation value with the threshold value after selecting the maximum correlation value.

Further, in the present invention an integration process of a correlation value is ended when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count set value, as recited in claims 56, 57, 60 and 61. Contrary to this, Higuchi compares the maximum correlation value with the threshold value. Furthermore, Higuchi fails to disclose or suggest that the correlation values obtained in the slots are integrated, as recited in claims 60 and 61 of the present invention.

Still further, the present invention has a feature of integrating correlation values obtained in the slots and comparing each of a calculated integrated correlation value with a reference set value, as recited in claims 58 and 59. Higuchi, however, appears to

only compare the maximum correlation value with the threshold value as mentioned above.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claims 53-60 is not anticipated within the meaning of 35 U.S.C. § 102.

As claims 2, 3 and 7 depend from claim 53, claims 10, 11, 14 and 16 depend from claim 54, claims 21-22 depend from claim 22, claims 24-27 depend from claim 56, claim 29 depends from claim 57, claims 31-32 and 35-38 depend from claim 58, and claim 43 depends from claim 60, Applicants respectfully submit that each of these claims incorporate the patentable aspects thereof, and are therefore allowable for at least the same reasons as discussed above.

Claim 51 was rejected under 35 U.S.C. § 102(e) as being anticipated by Ryu (U.S. Patent No. 5,995,434). By this Amendment, claim 51 has been cancelled and the subject matter incorporated into claim 52, thereby rendering the rejection moot.

Claims 13, 17, 18, 33, 39 and 46-48[1] were rejected under 35 U.S.C. § 103(a) as being unpatentable over Higuchi. In making this rejection, the Office Action took the position that Higuchi discloses all the elements of the claimed invention, with the exception of disclosing said first and second storage sections are provided in a single memory as recited in claim 13, an overflow notification section for notifying a shortage of storage area in at least one of said first and second storage sections when it occurs as recited in claim 17, a registration count notification section for notifying the number of correlation values stored in said first storage section as recited in claim 18, and a

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[1] It appears from the rejection that the Office Action is also rejecting claims 49 and 50.

register for arbitrarily setting said reference set value as recited in claims 33 and 39. The Examiner asserted that it would have been obvious to one of ordinary skill in the art to use a register for storing a reference set value to provide a means of quickly accessing the reference set.

With regard to claims 46-50, the Office Action took the position that it is well known in the art to perform data access during the refresh cycle of DRAM and would have been obvious to a person with ordinary skill in the art at the time of the invention to do so.

By this amendment, claim 46 has been cancelled and the subject matter incorporated into newly added claim 62. Claims 47 and 48 have been amended to depend there from.

Thus, as will be discussed below, Applicants respectfully submit that claims 13, 17, 18, 33, 39, 47-48, and 62-64 recite subject matter that is neither disclosed nor suggested by the prior art.

Claim 62 recites a communication synchronization apparatus for performing a cell search operation including a detection device that detects a correlation value between an input signal and a spreading code generated by the detection device, and detects a correlation peak value in a predetermined unit of slots. A dynamic RAM is provided as a memory used in said cell search operation.

Claim 63 recites a communication synchronization apparatus for performing a cell search operation including a detection device that detects each of several slots in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device, and the correlation values obtained in the slots are

integrated to detect a correlation peak value. A dynamic RAM is provided as a memory used for storing the integration results of correlation values.

Claim 64 recites a communication synchronization apparatus for performing a cell search operation including detection device that detects each of several slots in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device, and the correlation values obtained in the slots are integrated to detect a correlation peak value. A dynamic RAM is used as a memory in a correlator which detects correlation values in the slots in the manner of detecting the correlation value in each subunit obtained by dividing said spreading code, storing the correlation values in said memory, and outputting the sum of the correlation values of all subunits.

As described above, the present invention uses a dynamic RAM as a memory for the cell search operation, as recited in claims 62-64. The cell search detects a correlation peak value in a predetermined unit of slots.

Higuchi fails to disclose using a dynamic RAM (DRAM) as a memory. Thus, using dynamic RAM is not obvious for a person with ordinary skill in the art. SRAM had been conventionally used as a memory for the cell search operation as described generally in Applicants' specification at line 20, page 51 to line 24, page. Generally, in DRAM, a memory cell as an internal storage element is constructed by a capacitor. For this reason, contents stored in memory cells disappear unless the memory cells are recharged every predetermined period. The operation of charging the capacitors every predetermined period is called refresh, and the cycle is called a refresh cycle.

DRAMs requiring refresh are conventionally used as a main memory or expansion memory of a personal computer or workstation. More specifically, when a DRAM is used, a control construction for refresh is required in addition to memory cells, and the load of control is large. Conventionally, in consideration of disadvantages in maintaining data in memory cells, a compact mobile communication terminal such as a portable telephone uses not DRAM but SRAM that requires no refresh operation.

However, for example, when a scheme of integrating power values for several slots is used, as in the CDMA communication scheme, refresh control can be omitted by performing data access (the process of reading out power integration values up to the preceding slot from the DRAM, adding them to power values in the current slot supplied from the power conversion section, and writing the values) instead of refresh as a characteristic feature of the DRAM. In fact, since the time of one slot is 625 μsec and shorter than the refresh cycle, no refresh operation need be performed while integration is being performed.

As generally discussed in Applicants' specification, in the final cycle of integration, the peak is detected while performing addition by the adder 10,240 times, and the address of the DRAM corresponding to the peak point is stored in a static memory (e.g., an SRAM or a flip-flop not shown in Fig. 1). After that, the integration results at 10,240 points can disappear on the DRAM. Hence, no refresh operation need be performed even after the final cycle of integration.

In this exemplary embodiment of the present invention, the DRAM is used as a power value memory in the power value integration section. As is known in the art, the memory cells of the DRAM can have a much simpler structure than those of an SRAM.

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The DRAM 64 of this embodiment can also omit the refresh control construction that is normally necessary.

Hence, as a benefit of the claimed invention, the circuit area of the power value memory used for cell search can be largely reduced. Even in a portable terminal apparatus of wideband CDMA scheme requiring a relatively large memory capacity, the data memory can be realized with a size about 1/4 that of an SRAM conventionally used as a power value memory.

Since the conventional FDMA or TDMA communication scheme requires a not so large memory capacity, the circuit area rarely poses a problem even when an SRAM is used as the internal memory. To the contrary, the CDMA communication scheme requires a large memory capacity, and the circuit area becomes very large in use of an SRAM. The advantages of the present invention obtained by forming the internal memory using the DRAM are numerous.

As explained above, SRAM had been conventionally used as a memory for the cell search operation. Thus, it is not obvious for a person with ordinary skill in the art to use DRAM as a memory for the cell search operation as in the present invention.

Further, with respect to claims 13, 17, 18, 33 and 39, the Office Action has failed to provide any reference in support of the assertion of obviousness. Thus, it is submitted that this is impermissible hindsight.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claims 62-34, is not anticipated within the meaning of 35 U.S.C. § 103.

As claims 13, 17 and 18 depend directly or indirectly from claim 54, claims 33 and 39 depend from claim 58 and claims 47 and 48 depend upon claim 62, Applicants

respectfully submit that each of these claims incorporate the patentable aspects thereof, and are therefore allowable for at least the same reasons as discussed above.

Claim 52 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryu as applied to claim 51, and further in view of Tanaka et al. (U.S. Patent No. 6,011,709, "Tanaka").

In making this rejection, the Office Action took the position that Ryu discloses all the elements of the claimed invention except for disclosing that data access occurs in said dynamic RAM within its refresh cycle. Tanaka is cited for disclosing this limitation. By this amendment, claim 51 has been cancelled and the subject matter incorporated into claim 52. Thus, Applicants submit that the subject matter of claim 52 is neither disclosed nor suggested in any combination of the prior art.

Claim 52 recites a portable terminal apparatus wherein a dynamic RAM is used as a memory in a portable telephone having at least a function of voice communication through a radio channel and data access occurs in said dynamic RAM within a refresh cycle.

However, both Ryu and Tanaka fail to disclose the features of the present invention recited in claim 52. The Office Action asserted that it would be obvious to one of ordinary skill in the art to incorporate the use of coincident refresh and access cycles in Ryu, as taught by Tanaka to improve efficiency.

But, as discussed above in the discussion of DRAM, it would not have been obvious for a person with ordinary skill in the art that data access occurs in a dynamic RAM used as a memory in a portable telephone, within its refresh cycle for the same

Therefore, Applicants submit that Ryu and Tanaka, either alone or in

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combination, fail to disclose or suggest the present invention and it is respectfully submitted that the Applicants' invention, as set forth in amended claim 52, is not obvious within the meaning of 35 U.S.C. § 103.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 2-8, 10-19, 21, 22, 24-27, 29, 31-40, 43, 44, 47, 48 and 52-64 (claims 4-6, 8, 12, 15, 19, 34, 40 and 44 already being indicated as reciting allowable subject matter) and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108390-00002.**

Respectfully submitted,

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